A new source optimization approach for 2X node logic

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ABSTRACT

Source mask optimization (SMO) and double patterning technology (DPT) are considered key Resolution Enhancement Technique (RET) enablers for scaling 2x nodes and beyond design rules, using existing 193 nm ArF technology prior to EUV availability. SMO has been extensively shown to enlarge the process margin for critical layers in memory cells and test patterns; however the best SMO flow for a large random logic area up to full-chip application has been less explored. In this study, we investigated how the mask complexity in the source optimization impacts the final process window on a random logic layout after DPT, and proposed a new source optimization approach.
Example used is a contact layer for 2x logic designs. The SMO source optimization is performed using the SRAM cells with different mask complexities. These optimized sources are then evaluated based on a large-area random logic layout after mask-only optimization. CD variation through process window is used as the metric for comparison. We found the best result is obtained when the source is optimized with the full flexibility of the source and mask with freeform SRAFs and minimal MRC constraints. The source optimized with this approach can reduce CD variation through process window in the random logic without increasing its mask complexity.

Keywords: SMO, model-based SRAF, 20 nm node, double patterning, multi-patterning, optical lithography limit

1. INTRODUCTION

193 nm immersion lithography is expected to extend to sub 2x and even lower technology nodes.[1-2] Resolution Enhancement Techniques (RET), such as source mask optimization (SMO) and model-based sub-resolution assist features (SRAF) have been previously shown to improve the process margin and pattern fidelity compared with traditional source and mask.[3-7] While these RETs and hardware advances have significantly extended the capability of single-exposure, multi-patterning (MP) has become an inevitable solution as the pitch of critical layers fall below the optical resolution limit.[2] Aside from the process complexity and demand for high scanner overlay accuracy, MP also puts forward additional RET challenges. One example is that patterns of loose or forbidden pitches are frequently created after pattern splitting, which will negatively impact the depth of focus (DoF) margin. Also, MP results in an increase of the overall CD variation through process window[8]. With these challenges, it is important to use available RETs, such as SMO and DPT, in a coherent fashion to produce the most optimal solution without incurring a significant increase in production cost.

SMO has gained significant interest from both memory and logic chip makers, and has been shown to improve the process window and MEF for various patterns. Progress made in the hardware, such as the introduction of ASML's FlexRay illuminator, also enables the optimization solution to be quickly and reliably deployed in production without requiring the lead time for diffraction optical elements (DOE)[9]. FlexRay also allows for post-tape-out scanner tuning and matching. In past published studies, SMO has been mostly applied to repeating memory cells and test patterns[3-7,10-11], with less focus given to random logic for full-chip application[13]. This is mostly due to the fact that

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truly co-optimized SMO is computational intensive, and cannot be directly applied to the full-clip[5]. Therefore, the general approach is to optimize the source on the static random access memory (SRAM) cell and representative patterns from the larger logic patterns area, and then use the optimized source to do OPC on the full-clip design with model-based SRAF technology[13]. In this paper, we will explore a source optimization approach for SRAM cell and a random logic layout after DPT. In particular, the role of mask complexity in the source optimization is studied, and a new approach is proposed.

It has been previously shown that freeform SRAF provides better coverage for important diffraction orders, and thus yielding better results than conventional rectangular SRAF[10]. However, increased mask complexity with complex SRAF can significantly increase the shot count and potentially the cost in mask making. [10-11] The increased occurrence of isolated patterns or patterns with loose pitches after MP, gives lithographers more mask degrees of freedom using SRAFs, in particular more potential to benefit from freeform SRAFs, than single patterning (SP). This is especially important for dark-field layers such as contact and metal, due to its relatively low DOF and more complex pitch distribution. This paper discusses the importance of freeform SRAFs with source optimization in a 2x contact layer design, and its benefit to the large-area random logic without increased mask complexity.

SRAMs and logic circuits of 28, 22 and 20 nm are used in this investigation. The 28 nm node design can be achieved with single exposure, while the 22 and 20 nm node designs require double patterning. Both SMO and model based SRAF placements are performed by Tachyon SMO™. First, we analyze CD variation requirements for single and double patterning (DP), and identify DOF as the main root cause of CDU degradation with design rule scaling. Then, we will examine the importance of freeform SRAF in the source optimization, and propose a new source optimization approach. In this study, we use CD variation over the whole logic area and different process window conditions as a gauge to measure the performance of the source optimized with different mask complexities, and compare the new approach over the reference flow.

2. CDU performance towards 20 nm node

Figure 2.1 shows the SRAM and logic circuit pattern layouts used for this study. The memory cell is a 6-transistor SRAM with high pattern density.[3] The logic block is a combination of 4-standard cells, namely flip-flop, full-adder, inverter and NAND.[3] Both cells are designed for 28, 22 and 20 nm nodes in accordance with minimum pitch rules defined in table 2.1. Pattern splitting was implemented on 22 and 20 nm cells. In this work we will focus on the contact layer, i.e. the CD variation over the ~250 contact holes in the logic cell is used at metric.

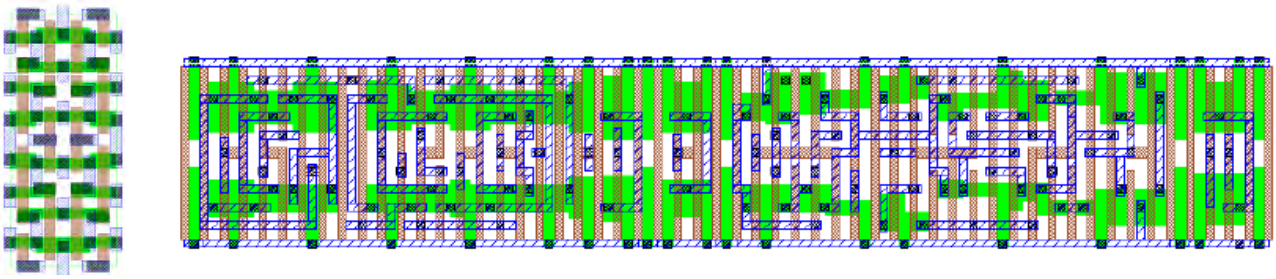

Fig. 2.1 SRAM and logic standard cells that were used in this study. The contact holes (black rectangular patterns) were evaluated in this study.

We used Tachyon SMO™ to optimize source and mask: First, the source and mask are co-optimized for the SRAM cell only. Second, based on this optimized source mask optimization, MO (mask optimization) was performed on the logic cell. Finally, CD's were extracted from simulated contours at 7 different process window conditions: (1) nominal condition, (2), (3) focus offset (+/-50 nm), (4), (5) dose offset (+/-3%) and (6), (7) mask CD error (+/-2 nm). The metric of CDU is defined as the 3-simga value of the overall process window (PW) CD variation.

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Table 2.1 Simulation condition for CDU estimation

Item:	Sub-item:	Condition:
Patterning condition	NA	1.35
	Wafer stack	Device stack
Mask	Film type	6% Att. PSM
	MRC	15 nm (Rectangular SRAF) 5 nm (Freeform SRAF)
	Mask tone	Clear field (Assuming negative tone development)
SMO	Resist model	Aerial image with blur
	SRAF	Rectangular, Freeform
Process error Assumption	Mask CD	+/-2 nm (1x)
	Dose	+/-3%
	Focus	+/-50 nm
Pattern pitch	28 nm	P_{gate} = 110 mm, P_{metal} = 90 nm
	22 nm	P_{gate} = 80 mm, P_{metal} = 80 nm
	20 nm	P_{gate} = 82 mm, P_{metal} = 64 nm

Figure 2.2 shows the simulated PW CD variations for the 28, 22 and 20 nm nodes on the logic standard cells after SMO. Even if we introduce DP, a degraded CDU is found in the case of 20 nm node. Figure 2.3 shows the budget breakdown of CD variation for the 3 technology nodes. This graph clearly shows that DoF is the most significant contribution to the overall CDU for both the 22 and 20 nm nodes. Or, in other words, the improvement of DoF is the most straight forward approach to improve the CDU performance.

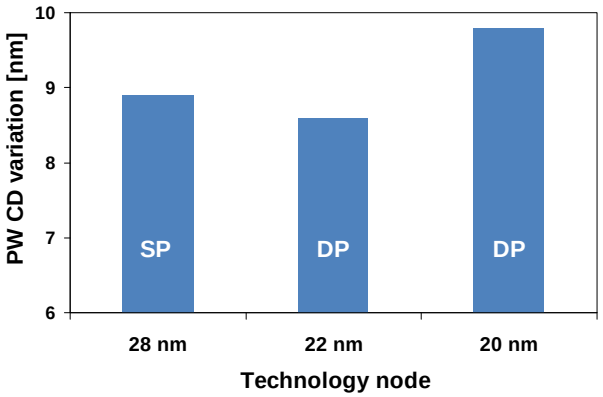

Fig. 2.2 Estimated PW CD variation for the three technology nodes. SP and DP were assumed for 28 nm and below 22 nm nodes respectively. Clear degradation of CD variation is found for the 20 nm node.

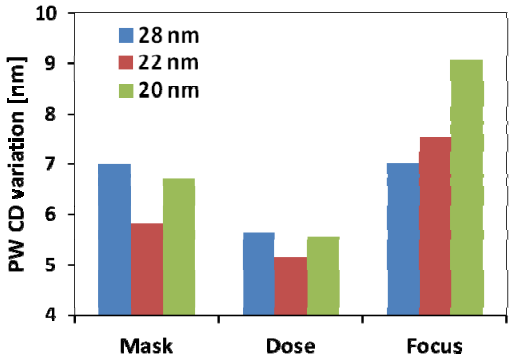

Fig. 2.3 Budget breakdown of PW CD variation for the three technology nodes. Focus is the common critical factor for CDU degradation in 22 and 20 nm nodes.

3. The impact of freeform SRAF

It is well known that properly placed SRAFs can significantly enhance the DoF[10]. Beside conventionally used rectangular SRAFs (Fig.3.1.a-1, b-1), freeform SRAFs, whose shape are not limited to rectangles, can be also used, as shown in Figure 3 for 28 nm and 22 nm SRAM cells. In this paper, freeform SRAFs are restricted to Manhattan

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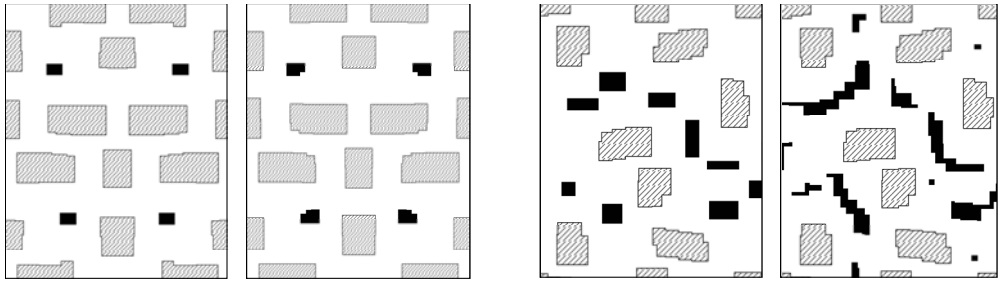
polygons. When the segments of SRAFs are sufficiently small, it can closely follow the curvature in the optimal region, and produces similar performance as non-Manhattan shapes. It is reported that freeform SRAFs can enable DoF improvement over rectangular SRAFs, especially in contact and metal layers, because they enable optimum diffraction light control by their flexible SRAF pattern shapes based on the illuminator.[6, 10]

DP requires a pattern split and thus introduces a larger physical area where SRAFs can be placed. Figure 3.1 shows the optimized masks of the SRAM patterns after SMO. Two groups of optimized SRAM patterns are shown: (a) single- and (b) double-patterning. For each group results with (1) rectangular SRAFs and (2) freeform SRAFs are shown. As clearly shown in Fig. 3.1, the optimized masks for rectangular and freeform SRAFs are not significantly different in the case of SP. On the other hand, there is a clear difference between rectangular and freeform SRAFs in the case of DP. We can thus expect that freeform SRAFs play a significant role in the improvement of overall process CD variation.



(a)-1 (a)-2 (b)-1 (b)-2

Fig. 3.1 Comparison of SRAF shapes: (a)-1 and -2 show the rectangular- and freeform-SRAF for SP (28 nm node) respectively. (b)-1 and -2 show the rectangular and freeform SRAFs and the optimized masks in case of DP for 22 nm node. For both technology nodes, 15 nm and 5 nm MRC was applied for rectangular SRAF and freeform SRAF respectively. The difference in SRAF shapes is insignificant in the case of SP but very clear in the case of DP.

In order to quantitatively compare the performance of different SRAF complexities, we simulated the DoF 6% of the exposure latitude (EL) and PW CD variation over 250 contact holes in the logic standard cells, based on the optimized source from the SRAM cells. The methodology to evaluate PW CD variation is described in section 2. Pattern data size after SMO was used as a measure of optimized mask complexity[8, 10]. Note that the estimation of the pattern data size was executed on the same pattern area for each technology node.

A clear DoF improvement is found with freeform SRAFs for 22 nm node after DP (Fig. 3.2). The population of contact holes with a DoF of less than 100 nm is halved with freeform SRAFs instead of rectangular SRAFs. Figure 3.3 shows that freeform SRAFs reduce PW CD variation by 10% over rectangular SRAFs. However, the gain in PW CD variation with freeform SRAF also incurs 25% increase in GDS file size, thus potentially an increase in mask making cost. This increase is attributed to the inherently larger mask pattern complexity of freeform SRAF. In conclusion, there is a trade-off between CDU vs. mask complexity. This trade-off is a negative aspect of the freeform SRAF technology.

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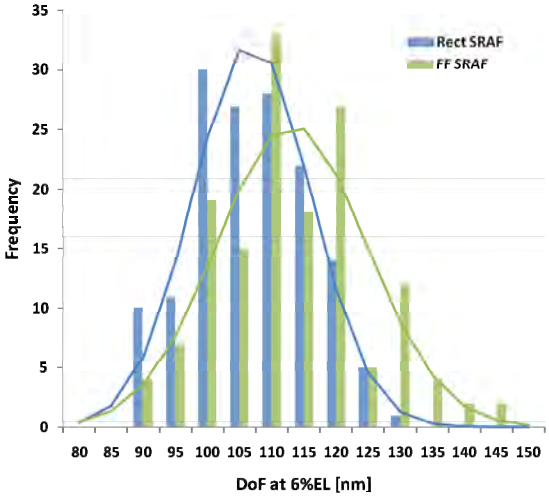

Fig. 3.2 DoF histogram of the 250 contact holes of the logic cell for (blue) rectangular- and (green) freeform-SRAFs. DoF is defined as the depth of focus at 6% exposure latitude. Freeform SRAFs clearly enhances the DoF compared to rectangular SRAFs.

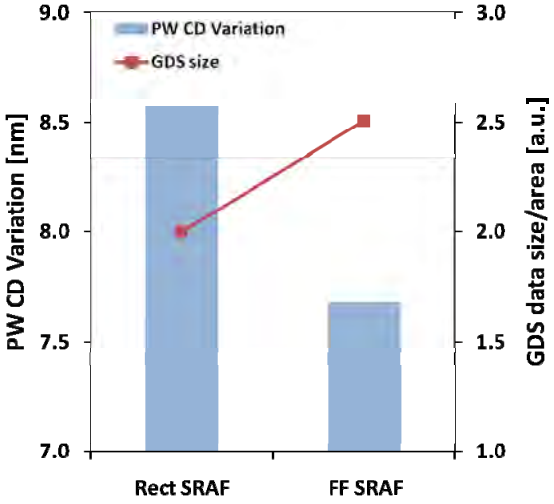

Fig. 3.3 Comparison of CD variation in rectangular- and freeform-SRAFs. Freeform SRAFs show a clear advantage for CDU. However, freeform SRAFs sacrifices mask complexity.

4. New source optimization approach

In this section, we explain the new SMO approach which we invented to overcome the CDU vs. mask complexity trade-off discussed in section 3. Fig. 4.1 shows the reference flow. First, SMO is implemented on the SRAM cell only. The input patterns used in this step are not necessarily limited to the SRAM cell, i.e. structures from the logic circuit block can be added if necessary. In the next step, MO is executed on the logic pattern. This part is essentially the same as conventional OPC. In order to avoid severe mask complexity or even unmanufacturable mask patterns, pragmatic mask constraints should be used, e.g. moderate mask restriction rules (MRC) as well as rectangular SRAF (see Fig. 4.1). If we can ignore the mask constraints, freeform SRAF can be adopted as indicated in Fig. 4.2. Of course this is not a realistic assumption when we consider mass-production.

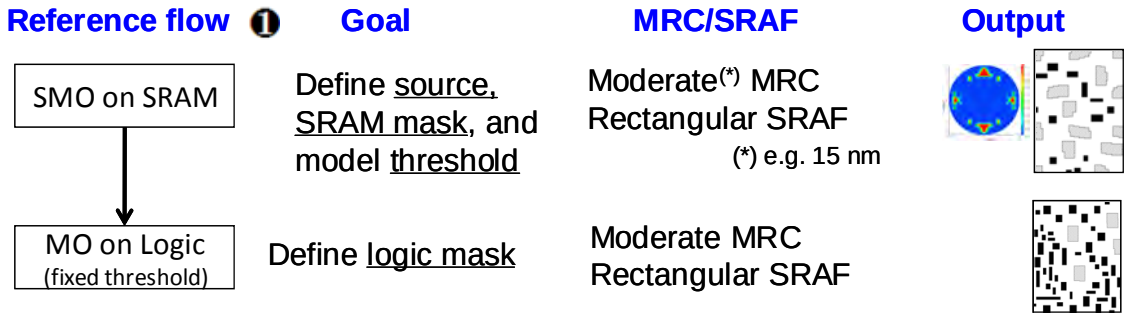

Fig. 4.1 Reference SMO flow. The purpose of the 1st step is to define source shape and define mask shape. Afterwards, mask only optimization (equivalent of conventional OPC) is implemented on logic patterns. Note that the outcome of the mask optimization step is used as pattern data for photomask fabrication. We therefore apply pragmatic mask restriction, i.e. 15 nm MRC and rectangular SRAFs.

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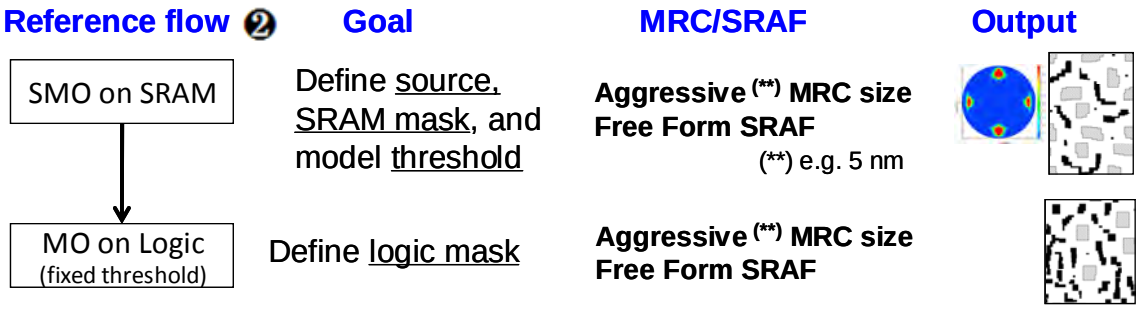

Fig. 4.2: Reference SMO flow with freeform SRAF's. The differences to the flow shown in Fig. 4.1 are the MRC and SRAF conditions. These less constrained mask conditions are expected to result in a better lithographic performance compared to the more constrained conditions of reference flow 1.

Fig.4.3 shows the new source optimization approach as we propose in this paper. The most outstanding difference compared with the reference flow is that in the new approach, SMO is first performed with freeform SRAF and aggressive MRC, whereas the final mask complexity of the SRAM and logic remains conservative. The initial SMO step is only to find the optimized source but here with minimal constraint from the mask side allowing full flexibility for the source. The subsequent two MO steps optimizes the mask for SRAM and logic, respectively, based on the optimized source with pragmatic (i.e. more restricted) mask setting. Note that the last step is identical to the reference flow 1 such that the final result is a physical mask with restricted mask constraints.

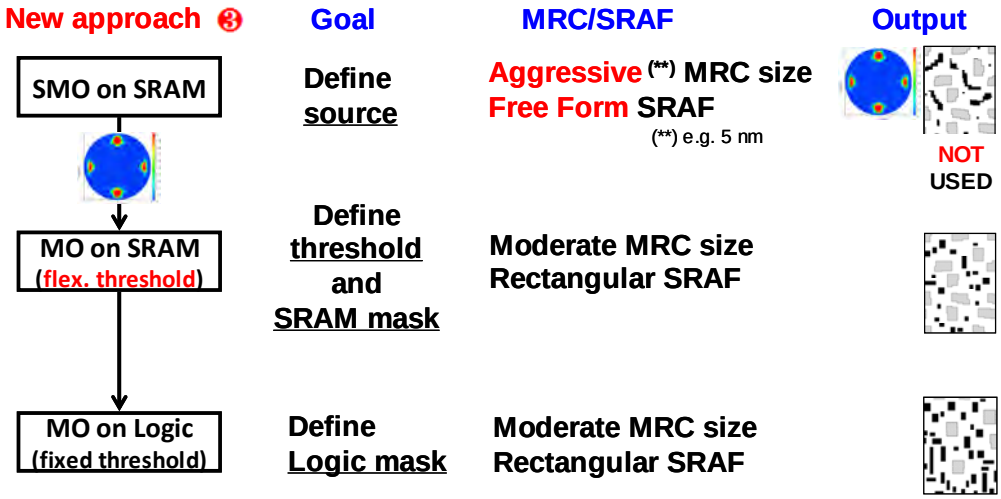

Fig. 4.3: The new source optimization approach. Unlike the reference flow, the source shape and SRAM mask optimization is executed in different steps. The mask extracted on the 1st step is not used in the next step; therefore, we can afford to apply unrealistic mask constraints during the source optimization step. For both the SRAM and the logic, the final mask shapes are defined by moderate MRC and are thus comparable to the final mask results of reference flow 1

The new approach shown in Fig.4.3 is expected to improve DoF because of the following reasons: The source shape is optimized with minimum mask restriction (for example 5 nm of MRC combined with freeform SRAFs). Therefore, the

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new approach gives the source much more freedom compared to the reference flow, where stricter mask constraints are applied during the source optimization. So, in case of the new approach a more optimal source shape can be extracted which, in a second step, can lead to a more optimal optimized mask with more pragmatic mask manufacturing constraints. Fig. 4.4 shows examples of optimized source and mask shapes in case of the reference flows with rectangular (a) and freeform SRAFs (b) and the new approach (c). Note that the source shapes are exactly the same in cases (b) and (c). In addition, the SRAF locations in (c) look relatively similar to the SRAF locations in (b) but are different from the locations in (a). We therefore expect the new approach to result in similar imaging performances compared to the case of freeform SRAFs.

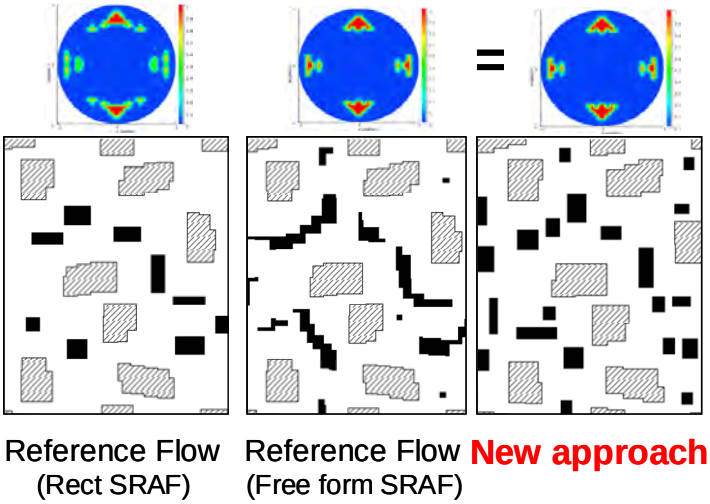

Fig. 4.4: Source and SRAM pattern shapes after SMO. (a), (b), and (c) correspond to reference flow with rectangular SRAF, reference flow with freeform SRAF and the new approach respectively. MRC size is 15 nm for rectangular SRAF, 5 nm for freeform SRAF.

5. Benefit of the new source optimization approach

We verified the benefit of the new source optimization approach in our circuit layout for the 22 and 20 nm nodes. We compared DoF of the reference flow 1 with the DoF of the new approach. Fig. 5.1 (a) shows the histograms of DoF at 6% EL of the logic layout. As can be seen in the figure, the new approach results in a clear DoF improvement, similar as was found for the use of freeform SRAF (see Fig.3.2). From Fig. 5.1 (a), the new approach reduces the number of contact holes with a DoF less than 100 nm from 21 to 9 within the area of inspection. In other words, the new approach enables to improve the DoF. We also compared the overlapping process window between both flows. The result is shown in Fig. 5.1(b). The figure clearly shows that the process window, and thus also the CDU, is improved when the new SMO approach is applied.

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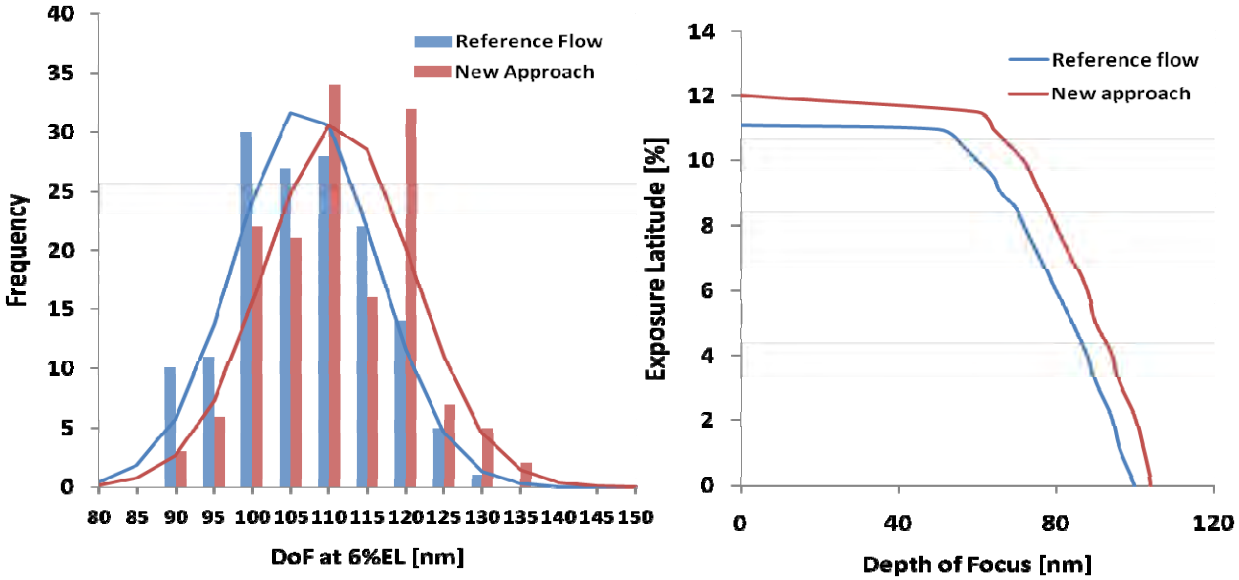

(a) (b)

Fig. 5.1: Comparison of process performance between the reference flow and the new approach. (a) and (b) show the histogram of DoF at 6% EL and the overlapping PW assuming CD +/- 4.6 nm respectively. The new approach results in a clear benefit with respect to the reference flow both for the DoF margin as well as the overlapping process window.

PW CD variation and pattern data size values for the reference flows 1 (rectangular assists) and 2 (freeform assists) and the new approach are shown in Fig. 5.2. The data clearly shows that the new approach realizes a similar level of PW CD variation to the reference flow with freeform SRAFs. Moreover, the reference flow with freeform SRAFs and the new approach offer smaller PW CD variation than that of the reference flow with rectangular SRAFs by 10% and 9% respectively. On the other hand, the pattern data size after applying the new approach remains the same as for the reference flow with rectangular SRAFs, i.e. a 0% data size increase was found for the new approach whereas an increase of 25% was found when freeform assists are used. In conclusion, the new SMO approach allows us to overcome the trade-off between CDU vs. mask complexity in the case of 22 nm node.

The next use case we investigated is the logic pattern of the 20 nm node. Except for the pattern pitch, there are 2 major differences compared to the 22 nm node: (1) we modified the SRAM layout by introducing a local interconnect layer and (2) a tighter mask CD specification is applied (1 nm instead of 2 nm). We applied these changes to avoid triple patterning of the contact hole layer. The modified 20 nm node SRAM layout is shown in Fig. 5.3.

Similar to the 22 nm node example, we used the PW CD variation as the metric to compare the performance of the source optimized with different mask complexities. We applied the new approach on the modified SRAM layout and simulated PW CD variation on the logic pattern. As can be seen from Fig. 5.4, the PW CD variation after applying the new approach successfully achieves a CDU performance comparable to the reference flow with freeform SRAFs and without the cost of increased pattern data size. The data suggests that the new SMO approach can also solve for this 20 nm node case the CDU vs. mask complexity trade-off. In summary, the new approach can be recognized as one of the promising candidates to achieve CDU improvement in case of double patterning.

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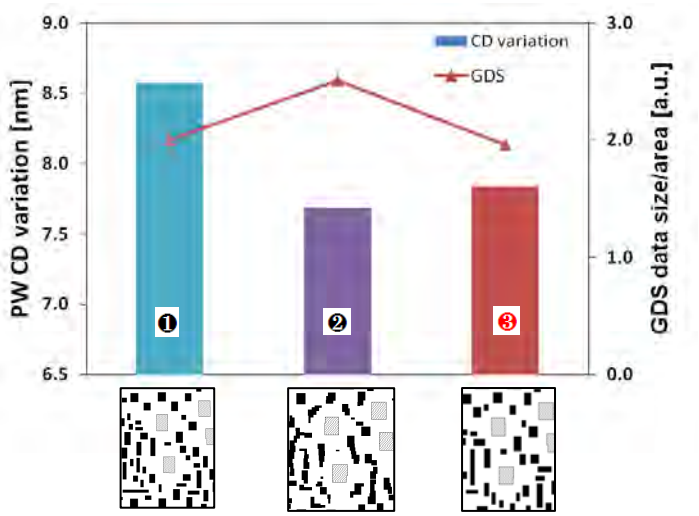

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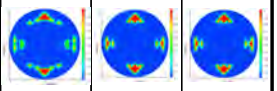
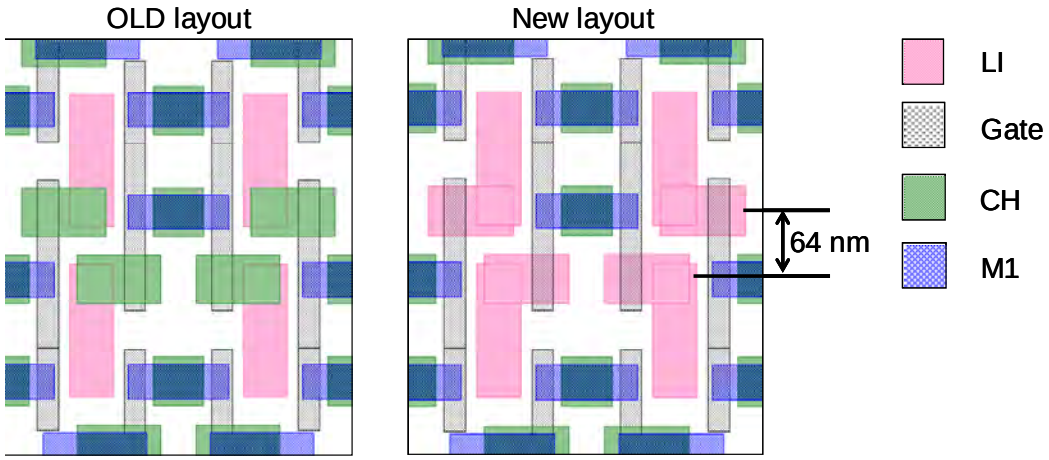
Flow	Reference		New
Source			
SRAF type	Rect	FF	Rect
MRC (nm)	15	5	15

Fig.5.2: Comparison of PW CD variation for 22 nm node with 3 types of SMO conditions. New approach (3) realizes comparable level of CD variation with freeform SRAF (2), however, there is no negative impact to mask complexity.



(a) (b)

Fig. 5.3 New SRAM layout implemented in 20 nm node. The difference between the old (a) and the new layout (b) is the gate contact. Some gate contact holes in the old layout are replaced by local interconnects in the new layout. Thanks to this operation, contact holes with minimum pitch are mitigated. However, it forces the local interconnect to adopt DP.

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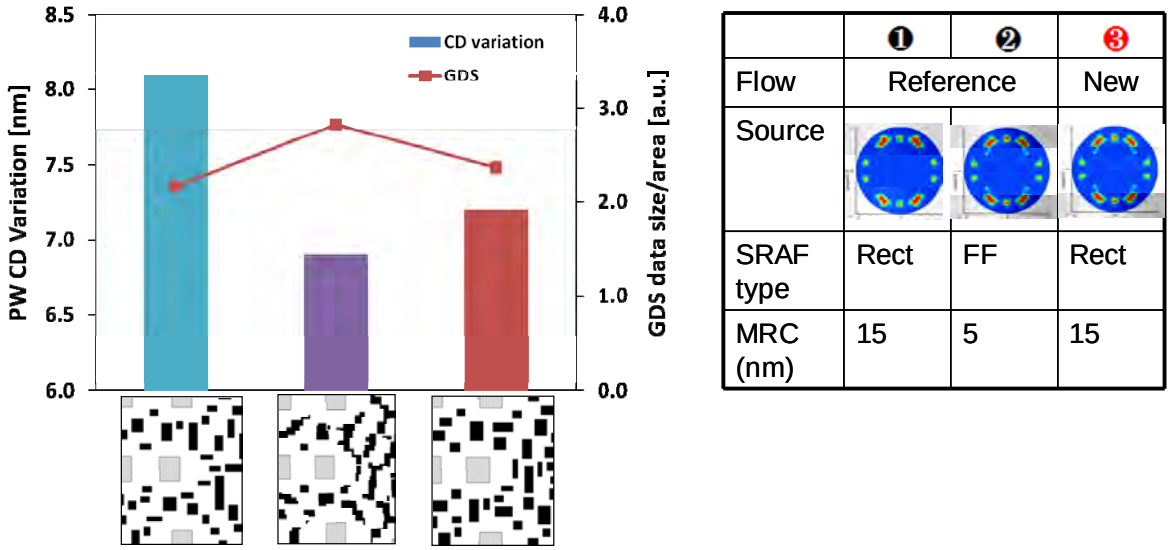

	❶	❷	❸
Flow	Reference		New
Source			
SRAF type	Rect	FF	Rect
MRC (nm)	15	5	15

Fig. 5.4 Comparison of PW CD variation in case of 20 nm node for 3 types of SMO flows. Similar as found for the 22 nm node, the new approach (3) allows solving the CDU vs. mask complexity trade-off.

6. CONCLUSION

We demonstrated a new source optimization approach for 2x nodes SRAM and random logic, which improves the process window and reduces CD variation through process window over the reference flow. In the new and reference approaches, SMO is performed on the SRAM cell only, and then mask-only optimization is applied on the random logic standard cell with the optimized source. The difference between the two approaches lies in the mask complexity allowed during the source optimization on SRAM. The reference flow uses rectangular SRAFs, while the new approach uses freeform SRAFs and minimal MRC. Rectangular SRAF is used for the mask-only optimization on the full logic layout in both flows to ensure mask manufacturability of the final result. This method is effective in that it gives the source full flexibility and maximum degrees of freedom when the mask is minimally constrained during the source optimization.

This approach yields comparable imaging quality with that of freeform SRAF while retaining pragmatic mask constraints. This is demonstrated on both 22 and 20 nm technology node designs. Firstly, we evaluate DoF improvement of the new approach, because it is the most critical factor on CDU degradation in both technology nodes. We find an improvement of both the overlapping process window and statistics of individual PW. The new approach also shows 10% improvement of PW CD variation for both technology nodes over the reference flow.

For the next step, we will apply this approach to larger logic pattern varieties and include both SRAM and logic for source optimization. Logic patterns will be selected by SMO Patten Selector for effective layout coverage.

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